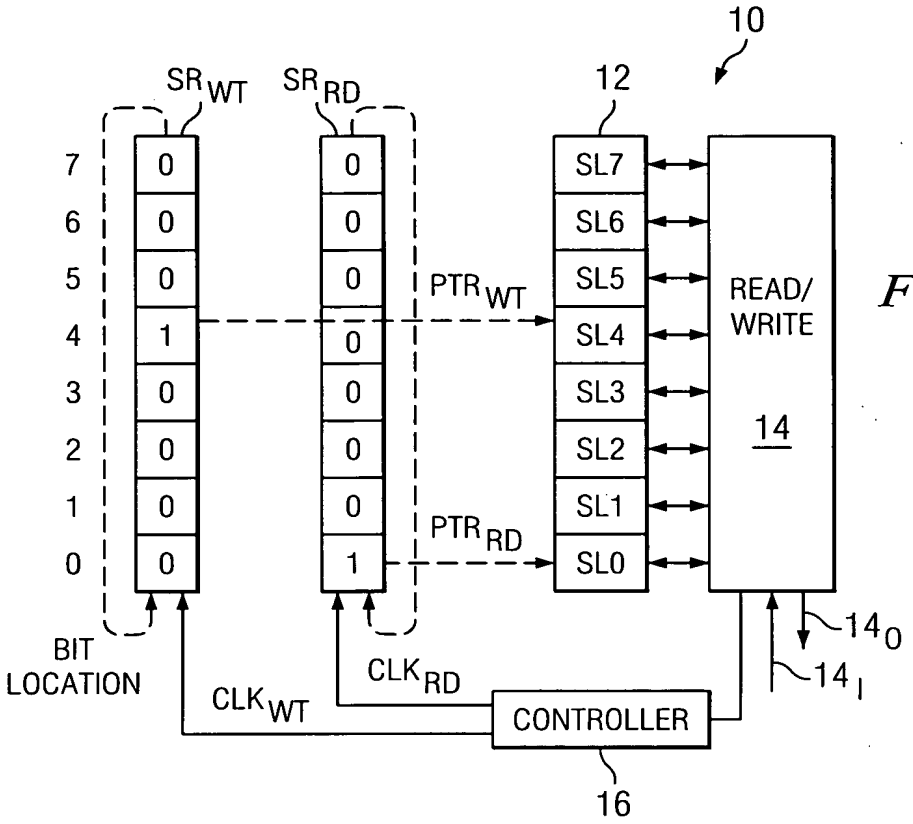
10
SR WT
SR RD
12
7
6
5
4
3
2
1
0
0
0
0
1
0
0
0
0
0
0
0
0
0
0
0
0
0
1
PTR WT
PTR RD
SL7
SL6
SL5
SL4
SL3
SL2
SL1
SL0
READ/
WRITE
14
14 0
14 1
BIT
LOCATION
CLK WT
CLK RD
CONTROLLER
16

FIG. 1a

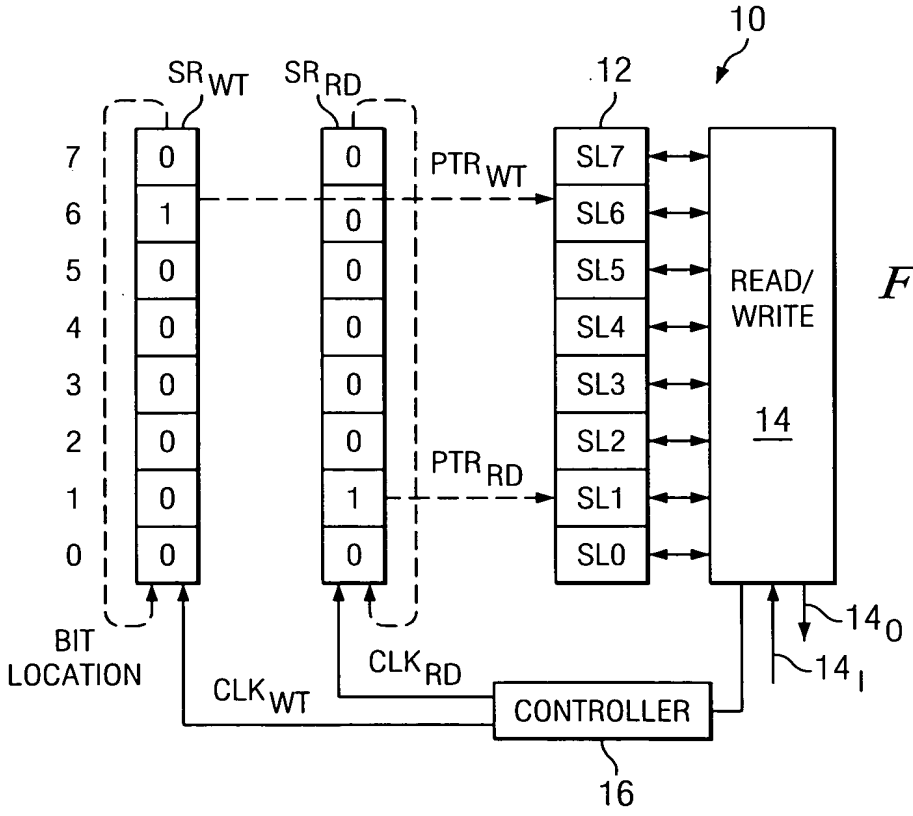
10
SR WT
SR RD
12
7
6
5
4
3
2
1
0
0
1
0
0
0
0
0
0
0
0
0
0
0
0
0
1
PTR WT
PTR RD
SL7
SL6
SL5
SL4
SL3
SL2
SL1
SL0
READ/
WRITE
14
14 0
14 1
BIT
LOCATION
CLK WT
CLK RD
CONTROLLER
16

FIG. 1b

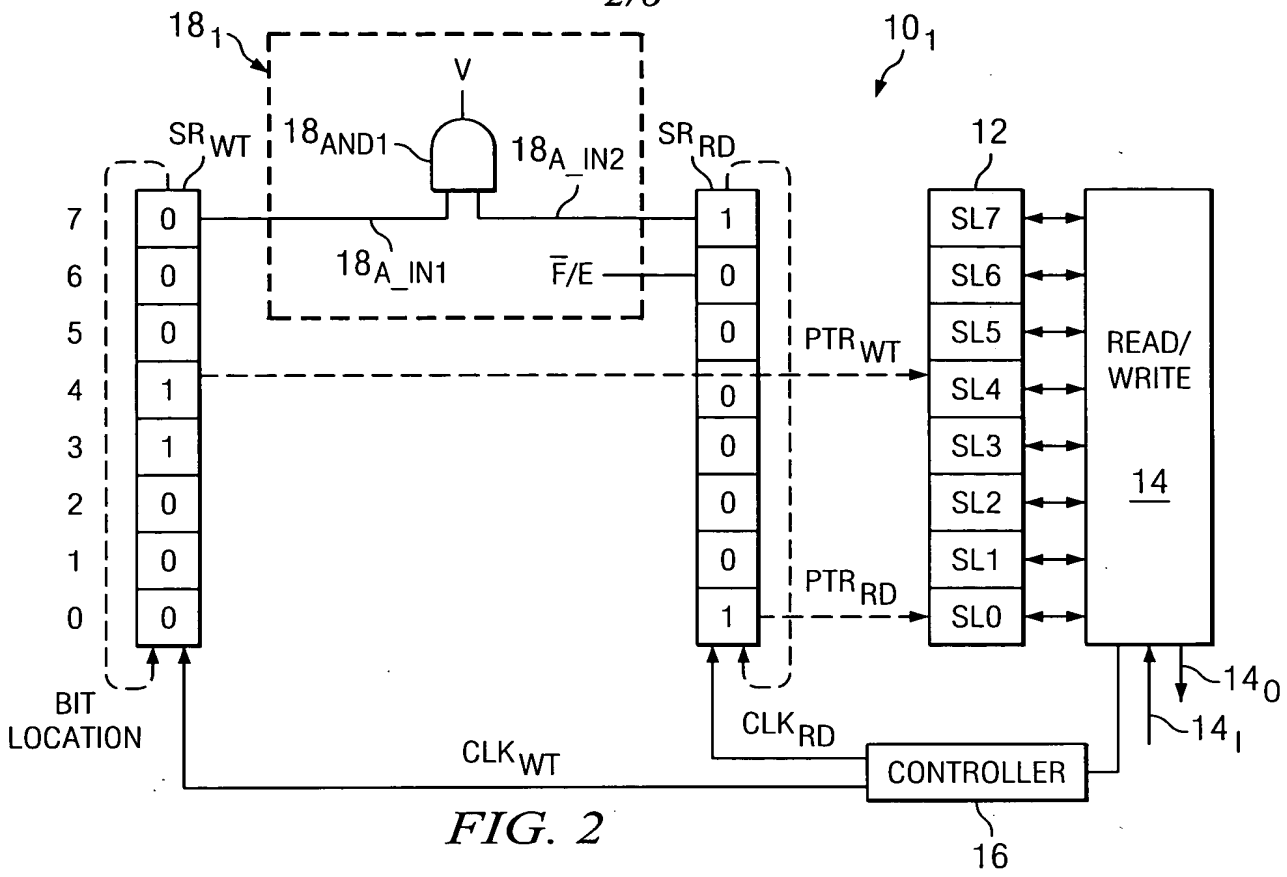

FIG. 2

BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	0	1	SR_{WT}
	0	0	0	0	0	0	1	1	SR_{RD_1}
	0	0	0	0	0	1	1	0	SR_{RD_2}
	0	0	0	0	1	1	0	0	SR_{RD_3}
	0	0	0	1	1	0	0	0	SR_{RD_4}
	0	0	1	1	0	0	0	0	SR_{RD_5}
	0	1	1	0	0	0	0	0	SR_{RD_6}
	1	1	0	0	0	0	0	0	SR_{RD_7}

FIG. 3

BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	0	1	SR_{RD}
	0	0	0	0	0	0	1	1	SR_{WT_1}
	0	0	0	0	0	1	1	0	SR_{WT_2}
	0	0	0	0	1	1	0	0	SR_{WT_3}
	0	0	0	1	1	0	0	0	SR_{WT_4}
	0	0	1	1	0	0	0	0	SR_{WT_5}
	0	1	1	0	0	0	0	0	SR_{WT_6}
	1	1	0	0	0	0	0	0	SR_{WT_7}

FIG. 4

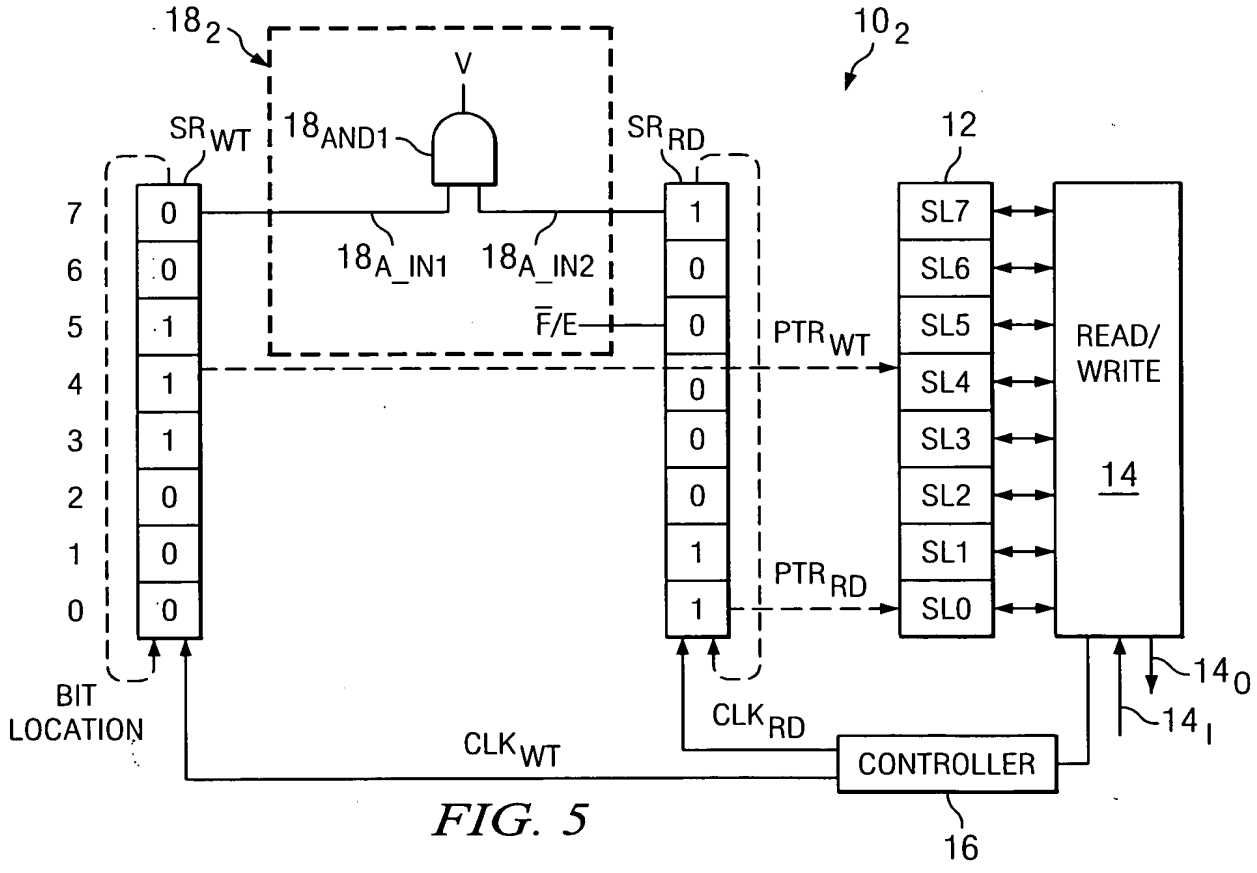

FIG. 5

BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	1	1	SR_{WT}
	0	0	0	0	0	1	1	1	SR_{RD_1}
	0	0	0	0	1	1	1	0	SR_{RD_2}
	0	0	0	1	1	1	0	0	SR_{RD_3}
	0	0	1	1	1	0	0	0	SR_{RD_4}
	0	1	1	1	1	0	0	0	SR_{RD_5}
	1	1	1	0	0	0	0	0	SR_{RD_6}

FIG. 6

BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	1	1	SR_{RD}
	0	0	0	0	0	1	1	1	SR_{WT_1}
	0	0	0	0	1	1	1	0	SR_{WT_2}
	0	0	0	1	1	1	0	0	SR_{WT_3}
	0	0	1	1	1	0	0	0	SR_{WT_4}
	0	1	1	1	0	0	0	0	SR_{WT_5}
	1	1	1	0	0	0	0	0	SR_{WT_6}

FIG. 7

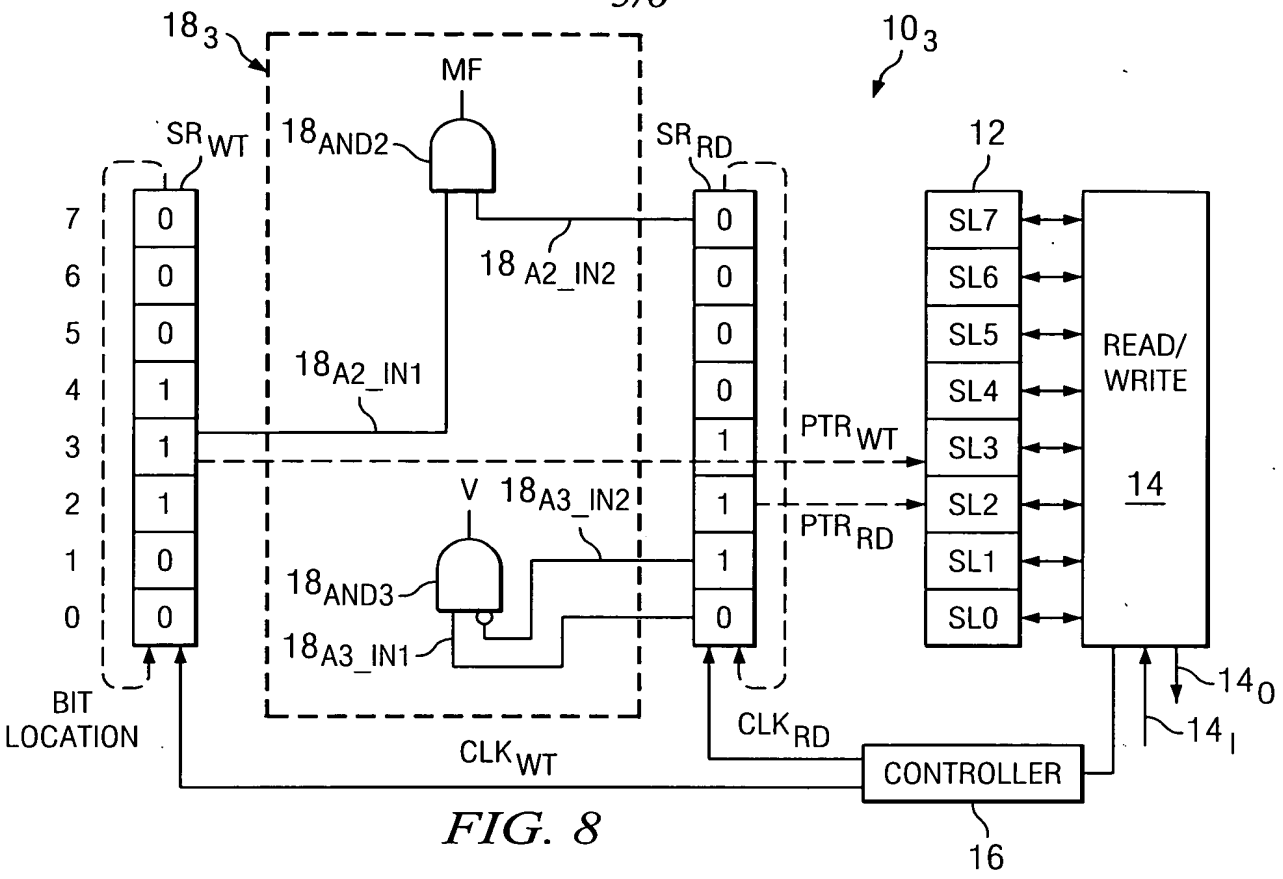

FIG. 8

BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	0	0	0	1	1	1	0	0	SR_{WT}
	0	0	0	0	1	1	1	0	SR_{RD_1}
	0	0	0	1	1	1	0	0	SR_{RD_2}
	0	0	1	1	1	0	0	0	SR_{RD_3}
	0	1	1	1	0	0	0	0	SR_{RD_4}
	1	1	1	0	0	0	0	0	SR_{RD_5}
	1	1	0	0	0	0	0	1	SR_{RD_6}
	1	0	0	0	0	0	1	1	SR_{RD_7}
	0	0	0	0	0	1	1	1	SR_{RD_8}

FIG. 9

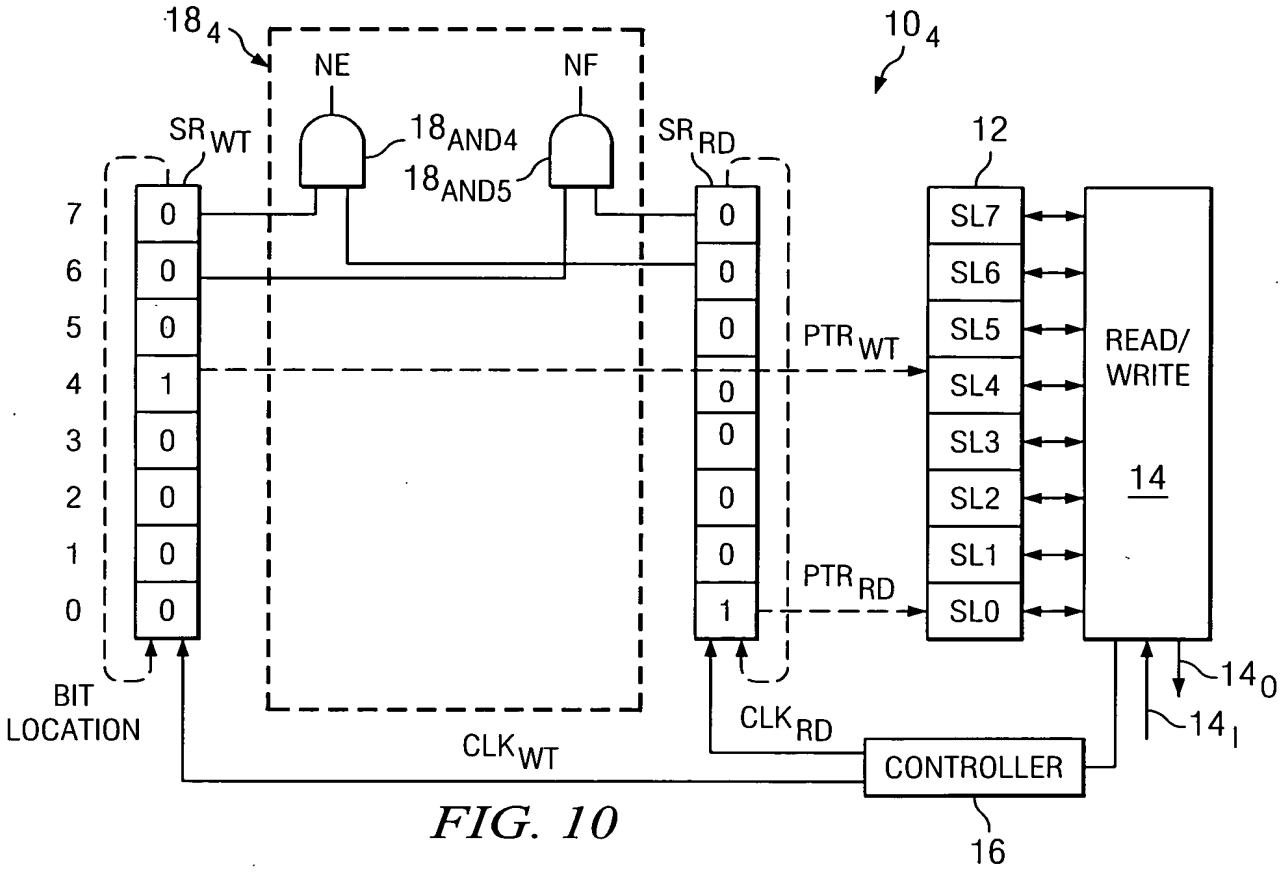
18_4
NE
NF
10_4
SR_{WT}
18_{AND4}
18_{AND5}
SR_{RD}
12
7
6
5
4
3
2
1
0
0
0
0
1
0
0
0
0
0
0
0
0
0
0
0
0
0
1
SL7
SL6
SL5
SL4
SL3
SL2
SL1
SL0
PTR_{WT}
PTR_{RD}
READ/
WRITE
14
14_0
14_1
BIT
LOCATION
CLK_{WT}
CLK_{RD}
CONTROLLER
16

FIG. 10